What is claimed is:

1. A method for connecting at least one high speed integrated circuit chip ("IC") to external terminals, said IC having a plurality of signal pads, said method comprising:

providing a substrate;

forming a plurality of microstrips on said substrate,

said plurality of microstrips for providing transmission between said plurality of signal pads and said external terminals,

at least a pair of said plurality of microstrips for transmitting signals from or to said IC,

said pair of said plurality of microstrips ("said pair of microstrips") for being capacitively coupled to each other, through a first partial length,

said pair of microstrips for having substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips.

2. The method of claim 1, wherein said pair of microstrips has a width that increases as it is outwardly routed.

3. The method of claim 1, wherein a width of each of said pair of microstrips along said first partial length is less than a width determined from an equation 50 ohm = 1 / vC, where v is a velocity of propagation of the signals and C is a capacitance per unit length.

4. The method of claim 1, wherein said substrate is made of substantially Alumina.

5. The method of claim 1, wherein said IC is a demultiplexor or multiplexor chip for OC-768 applications.

6. The method of claim 1, wherein said signals comprise high-speed data signals operating at a frequency of at least 20 Gbps.

7. The method of claim 1, wherein said external terminals comprise a pair of coaxial terminals.

8. The method of claim 1, wherein said first partial length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from said IC.

9. The method of claim 1, wherein a second partial length within said first partial length of said pair of microstrips is widened to increase its capacitance.

10. The method of claim 9, wherein said second partial length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from said IC.

11. The method of claim 7, wherein a second partial length within said first partial length of said pair of microstrips is widened to increase its capacitance.

12. The method of claim 1, wherein a width of each of said pair of microstrips along a portion of said first partial length is not more than 5 mils,

wherein spacing between said pair of microstrips along a portion of said first partial length is not more than 5 mils.

13. The method of claim 1, wherein said pair of microstrips is substantially 50-ohm transmission lines throughout substantially the entire length of said pair of microstrips.

14. The method of claim 1, wherein said signals are differential signals.

15. The method of claim 1, wherein said substrate is a single-layer substrate.

16. The method of claim 1, wherein said substrate is a multiple-layer substrate.

17. The method of claim 7, wherein a width of a dielectric ring portion of one of said pair of coaxial terminals is substantially identical to a thickness of said substrate.

18. The method of claim 1, wherein said external terminals comprise GPPO connectors.

19. The method of claim 7, wherein a width of a dielectric ring portion of one of said pair of coaxial terminals is substantially identical to a thickness of said substrate.

20. The method of claim 1, wherein said pair of microstrips are for transmitting high-speed signals,

wherein said plurality of microstrips further comprise a second plurality of microstrips

that are for transmitting low speed signals.

21. A method forming a package for connecting at least one high speed integrated circuit chip ("IC"), said IC comprising at least one high speed signal and low speed signals, said method comprising:

providing a substrate to mount said IC;

forming at least one external coaxial connector for communicating said high-speed signal,

forming an array of terminals at a bottom side of said substrate for communicating at least said low speed signals;

selectively forming a plurality of first microstrips on a top surface of said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and said array of terminals;

selectively forming a plurality of interconnections within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least one terminal of said array of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector.

22. The method of claim 21, wherein a rate of said high speed signal is at least 20 Gbps, and a rate of one of said low speed signals is lower than 20 Gbps.

23. The method of claim 21, wherein said at least another one of said plurality of first microstrips is for providing substantially constant characteristic impedance,

wherein at least one of said plurality of interconnections is for providing substantially constant characteristic impedance throughout said at least one of said plurality of

interconnections connecting at least said at least another one of said plurality of first microstrips to at least one terminal of said array of terminals.

24. The method of claim 21, wherein said at least one external coaxial connector is placed on a side of said substrate.

25. The method of claim 21, said high-speed signal does not transmit through said substrate.

26. The method of claim 21, wherein said at least one external coaxial connector comprises a GPPO connector.

27. The method of claim 21, wherein said array of terminals comprises ball grid array ("BGA") terminals.

28. The method of claim 21, wherein said substrate comprises at least a first dielectric layer and a second dielectric layer.

29. The method of claim 21, wherein said substrate comprises a plurality of dielectric layers formed by a low-temperature co-fired ceramics process, not a printed circuit board.

30. The method of claim 21, wherein said substrate comprises a plurality of dielectric layers formed by a high-temperature co-fired ceramics process.

31. The method of claim 21, wherein said substrate is ceramic.

32. The method of claim 21,

wherein one of said plurality of interconnections comprises a via connection,

wherein said via connection comprises a conductor core for a signal,

wherein said conductor core is surrounded by a dielectric material portion of said substrate and bound by a circular opening for a ground signal.

33. The method of claim 21,

wherein said step of selectively forming a plurality of first microstrips comprises:

forming at least a pair of co-planar ground lines on both sides of said at least one of said plurality of first microstrips ("high-speed microstrip");

wherein both of said co-planar ground lines are for being capacitively coupled to said high-speed microstrip through a first partial length.

34. The method of claim 33, further comprising:

widening said high-speed microstrip through a second partial length to increase its capacitance.

35. The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of selectively forming a plurality of interconnections comprises:

selectively forming a plurality of second paths between said first and second dielectric layers;

selectively forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein said via connection is underneath said at least one of said plurality of first microstrips;

wherein said at least one of said plurality of second paths and said at least one of said plurality of third paths form a continuous ground path.

36. The method of claim 35,

wherein said at least one of said plurality of second paths is for providing substantially constant characteristic impedance along said at least one of said plurality of second paths;

wherein said via connection is for providing substantially constant characteristic impedance along said via connection;

wherein said at least one of said plurality of third paths is for providing substantially constant characteristic impedance along said at least one of said plurality of third paths.

37. The method of claim 35, further comprising:

tapering out said at least one of said plurality of first microstrips at a tapering section,

wherein said via connection is underneath said tapering section.

38. The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of selectively forming a plurality of interconnections comprises:

selectively forming a plurality of second transmission lines between said first and second dielectric layers;

selectively forming a plurality of third transmission lines at a bottom of said second dielectric layer,

selectively forming a plurality of first via connections in said first dielectric layer, and

selectively forming a plurality of second via connections in said second dielectric layer,

wherein one of said plurality of first via connections connects said at least another one of said plurality of first microstrips to one of said plurality of second transmission lines,

wherein one of said plurality of second via connections connects said one of said plurality of second transmission lines to one of said plurality of third transmission lines,

wherein said one of said plurality of first via connections is aligned with said one of said plurality of second via connections.

39. The method of claim 21,

wherein said at least one of said plurality of first microstrips comprises a first partial length near an inner edge of said substrate and a second partial length toward an outer edge of said substrate,

wherein a width along said second partial length is wider than a width along a portion of said first partial length.

40. The method of claim 39,

wherein said first partial length comprises a third partial length and a fourth partial

length,

wherein said third partial length is closer to said inner edge than said fourth partial length is to said inner edge,

wherein a width along said third partial length is wider than a width along said fourth partial length.

41. The method of claim 21,

wherein said substrate comprises at least a first dielectric layer, a second dielectric layer, and a third dielectric layer

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of selectively forming a plurality of interconnections comprises:

selectively forming a plurality of second paths between said first and second dielectric layers;

selectively forming a plurality of third paths between said second and third dielectric layers;

selectively forming a plurality of fourth paths at a bottom of said third dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of fourth paths through at least a first via connection and a second via connection;

wherein said at least another one of said plurality of first microstrips is connected to one of said plurality of third paths,

wherein spacing between said first via connection and said second via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

42. The method of claim 41,

wherein spacing between said first via connection and said one of said plurality of third paths is about half of a separation between said at least one of said plurality of second paths and a said at least one of said plurality of fourth paths.

43. The method of claim 21, wherein said substrate is less than 0.4 cubic inches.

44. The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein said top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of selectively forming a plurality of interconnections comprises:

selectively forming a plurality of second paths between said first and second dielectric layers;

selectively forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein a first portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of second paths,

wherein a second portion of said at least one of said plurality of first microstrips is over said via connection,

wherein a third portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of third paths,

wherein said first portion is narrower than said third portion,

wherein said second portion tapers out from said first portion toward said third portion,

wherein said first portion, said second portion and said third portion are for providing substantially constant impedance along said first portion, said second portion and said third portion.

45. The method of claim 32,

wherein said via connection's impedance is determined by:

$$60 \log (b/a) / [\eta \times \varepsilon]$$

wherein b is a diameter of said circular opening, a is a diameter of said conductor core, ε

is a dielectric constant of said dielectric material portion, and η is an efficiency of a capacitance between said circular opening and said conductor core as compared to that in a coaxial cable having same a and b dimensions.

46. A method for making a connection package for connecting a plurality of signals of at least one broadband high-speed integrated circuit chip ("IC") to a plurality of external terminals, comprising:

providing a substrate comprising a plurality of dielectric layers;

selectively forming a plurality of microstrips on top of said substrate, at least one of said plurality of microstrips ("high-speed microstrip") being disposed to conduct a high speed signal between said IC and one of said plurality of external terminals;

selectively forming at least a pair of co-planar ground strips on top of said substrate and on both sides of said high-speed microstrip, a partial length of said pair for being capacitively coupled to a first partial length of said high-speed microstrip;

selectively forming a first ground plane at a first vertical distance below said high-speed microstrip in said substrate;

selectively forming a second ground plane at a second vertical distance below said high-speed microstrip in said substrate;

selectively forming at least one via connector to connect said first and second ground planes;

selectively forming a plurality of internal striplines in said substrate, said plurality of internal striplines for connecting signals between said IC and a second set of external terminals;

selectively forming a plurality of internal coaxial connectors in said substrate, being adapted to connect said plurality of internal striplines through said substrate.

47. The method of claim 46, further comprising:

widening said high-speed microstrip through a second partial length while maintaining its capacitance.

48. The method of claim 46, further comprising:

forming said at least one via connector below said high-speed microstrip.

49. The method of claim 46, wherein said one of said plurality of external terminals connected to said high-speed microstrip is a coaxial GPPO connector.

50. The method of claim 46, wherein said second set of external terminals are BGA connectors.

51. The method of claim 46, wherein said high-speed microstrip is capable of carrying a signal at a rate of at least 30 Gbps.

52. The method of claim 46, further comprising:

forming at least a pair of said plurality of microstrips to connect a pair of high-speed differential signals.

53. A method for forming a connection package for connecting a plurality of signals of at least one high-speed integrated circuit chip ("IC"), comprising:

providing a substrate comprising a plurality of dielectric layers;

mounting a plurality of coaxial terminals to a side of said connection package;

mounting a plurality of BGA terminals mounted to a bottom of said connection package;

selectively forming a plurality of microstrips on a first layer of said plurality of dielectric layers, being disposed to connect to said plurality of signals,

some of said plurality of microstrips ("first microstrips") for connecting some of said plurality of signals ("first signals") to said plurality of coaxial terminals;

selectively forming a plurality of internal connections on a second layer of said plurality of dielectric layers;

selectively forming a plurality of inter-layer connections in said substrate,

said plurality of inter-layer connections connecting some of said plurality of microstrips ("second microstrips") to said plurality of internal connections and connecting said plurality of internal connections to said plurality of BGA terminals.

54. The method of claim 53,

wherein said plurality of microstrips comprise a pair of high speed differential signals and three co-planar ground strips, said pair of high speed differential signals for being capacitively coupled to said three co-planar ground strips through a first partial length;

wherein said pair of high speed differential signals are widened in width from an inner edge of said substrate to an outer edge of said substrate, said pair of high speed differential signals for maintaining their capacitance substantially constant.

55. The method of claim 53,

wherein said step of selectively forming a plurality of internal connections comprises:

forming internal striplines to connect active signals; and

forming ground strips to connect to ground;

wherein said step of selectively forming a plurality of inter-layer connections comprises:

forming internal coaxial conductors to connect active signals;

forming via connectors to connect to ground.

56. The method of claim 53, a path throughout substantially said first microstrips and said plurality of coaxial terminals for providing substantially constant impedance,

wherein a rate of said first signals is at least 20 Gbps.

57. A method comprising:

providing a substrate;

forming a plurality of coaxial terminals located substantially at a first outer edge of said substrate;

forming a plurality of non-coaxial terminals located substantially at a second outer edge of said substrate;

forming a plurality of microstrips on said substrate;

a pair of said plurality of microstrips ("pair of microstrips") having a first length near an inner edge of said substrate and a second length near said first outer edge of said substrate, said pair of microstrips connected to said plurality of coaxial terminals;

said pair of microstrips for providing capacitive coupling to each other at said first

length,

said pair of microstrips for carrying active signals,

said pair of microstrips for substantially eliminating capacitive coupling to each other at said second length,

each of said pair of microstrips having a first width at said first length, each of said pair of microstrips having a second width at said second length, said second width being greater than said first width,

said pair of microstrips for providing substantially constant characteristic impedance throughout substantially said pair of microstrips and said plurality of coaxial terminals,

some of said plurality of microstrips connected to said plurality of non-coaxial terminals;

wherein a distance between said pair of microstrips at said second length is greater than a distance between said pair of microstrips at said first length.

58. The method of 57, further comprising:

widening said pair of microstrips in width along a third length within said first length.

59. The method of 57, wherein a width of an inner conductor of each of said plurality of coaxial terminals is substantially identical to a width of each of said pair of microstrips at said second length.